

TSMC-01-658



March 22, 2002

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To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572
20 McIntosh Drive
Poughkeepsie, N.Y. 12603

RECEIVED
APR 9 - 2002
TC 1700

Subject: | Serial No. 10/043,483 01/11/02 |
| Willys Choi |
| UPSIDE DOWN BAKE PLATE TO MAKE |
| VERTICAL AND NEGATIVE PHOTORESIST |
| PROFILE |
Grp. Art Unit: 1756

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.

The following Patents and/or Publications are submitted to
comply with the duty of disclosure under CFR 1.97-1.99 and
37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being
deposited with the United States Postal Service as first class
mail in an envelope addressed to: Commissioner of Patents and
Trademarks, Washington, D.C. 20231, on April 1, 2002.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

SB Ackerman 4/1/02

U.S. Patent 5,849,435 to Akram et al., "Method for Forming a Thin Uniform Layer of Resist for Lithography," discloses a process, which inverts a wafer with resist and then hardens.

U.S. Patent 6,100,506 to Colelli, Jr. et al., "Hot Plate with In Situ Surface Temperature Adjustment," discloses a photoresist bake using a right side up hot plate.

U.S. Patent 5,578,127 to Kimura, "System for Applying Process Liquid," discloses a coat and bake photoresist system.

The following two U.S. Patents disclose processes with bakes and hot plates:

- 1) U.S. Patent 4,800,251 to Matsuoka, "Apparatus for Forming a Resist Pattern."
- 2) U.S. Patent 5,877,076 to Dai, "Opposed Two-Layered Photoresist Process for Dual Damascene Patterning."

Sincerely,



Stephen B. Ackerman,
Reg. No. 37761